Conference Theme: Integrated Circuits for Intelligent Systems

We are now witnessing many types of intelligent systems coming around the corner. Equipped with new technologies such as the Internet of things, deep learning, big data analysis, cloud computing, and so forth, everyday life is expected to drastically change with conveniences such as automatic driving on electric cars, fast online shopping with drone delivery, vast knowledge base exceeding human intelligence, autonomous robots in hazardous environment and so on. Behind all these lurk fast-pace integrated circuits, which provide continually ever higher levels of functionality, connectivity, and energy efficiency.

The IEEE A-SSCC 2016 (Asian Solid-State Circuits Conference) is an international forum for presenting the most updated and advanced chips and circuit designs in solid-state and semiconductor fields. The conference is supported by the IEEE Solid-State Circuits Society and will be held in Asia. Further details on the conference and paper submission guidelines and templates will be available at the A-SSCC official website http://www.asscc.org/ around the beginning of April, 2016.

Paper Submission
Prospective authors are invited to submit full-length, four-page manuscripts, including figures, tables and references, to the official A-SSCC 2016 website. All papers will be handled and reviewed electronically. Papers are solicited in the following categories:

Regular Session
1. Analog Circuits & Systems: Amplifiers, comparators, switch capacitor circuits, continuous-time & discrete-time filters, voltage/current references; DC-DC converters, power-control circuits; IF/baseband analog circuits, AGC/VGA; non-linear analog circuits.
2. Data Converters: Nyquist-rate and oversampling A/D, D/A converters, time-to-digital converters, and capacitance-to-digital converters; sub-circuits for data converters including sample-and-hold circuits, calibration circuits, etc.
4. SoC & Signal Processing Systems: System-on-chip(including 3D integration), microprocessors, network processors, baseband communication processing system & architectures, energy efficient signal-processing systems; multimedia and recognition processing systems; cryptographic and security-processing circuits and systems; bio-medical/neural signal processors and sensor network systems.
5. RF: Receivers/transmitters/transceivers for wireless systems; narrowband RF, ultra-wideband and millimeter-wave circuits; circuits and building-blocks including RF front-end, LNA, mixer, power amplifiers, VCOs, frequency synthesizers, RF filters, RF switches, power detectors, active antennas.
6. Wireline: Receivers/transmitters/transceivers for wireline systems; optical/electrical data links and backplane transceivers; power-line communication; clock generation circuits, PLL, DLL, spread-spectrum clock generation; building blocks for high-speed wireline communication; analog-digital mixed-mode circuits.
7. Emerging Technologies and Applications: Advanced system designs and circuit solutions for technologies and applications including state-of-the-art devices and packaging technologies; flexible and printable electronics; smart sensors and transducers; MEMS for analog, RF, and sensor applications; image sensors and displays; energy harvesting systems; transceiver systems; medical/bio-electronics/bio-inspired chip design and silicon systems.
8. Memory: Volatile and Non-volatile memory: new memory designs for 3D/2D architectures, emerging devices such as resistive-phase change/magnetic-/ferro-electric-memory devices; data storage and multi-bit-cell memory design; cache-memory system, multi-port memory, and CAM design; yield-enhancing and ECC techniques; memory testing and built-in-self-test.

Special Session
1. Industry Program: This special category accepts only papers based on state-of-the-art industrial products. Strong emphasis on systems realized by silicon chips is encouraged. The papers should cover architecture, circuits, process technology, packaging and testing, including characterization results, die and system photos, as well as product demos.
2. Student Design Contest: A student design contest is held among the accepted papers with system prototypes or measurement results of which operations can be demonstrated on-site. Refer to the web for further information.

Papers related to integrated circuits for intelligent systems are highly solicited. Papers on low-power and/or low-voltage approaches, signal integrity, noise, test, and manufacturability for all the above categories are welcomed. Measurement results are highly recommended, especially for analog, and RF categories. Design methodologies for SIP, and SoC are included in the scope of the conference; the papers only describing CAD tools and CAD algorithms are not considered. Authors must follow detailed instructions provided within the “Authors" section of the website, including the Authors’ Guide and Pre-publication Policy. The technical content beyond the abstract of the accepted paper must not be announced, published, or in any way put in the public domain prior to the Conference. Extended versions of selected papers from the Conference will be published in a Special Issue of the IEEE Journal of Solid-State Circuits.

Important dates

- **Submission deadline**: June 20, 2016, 20:00 (GMT)
- **Acceptance notification**: Aug. 5, 2016
- **Final paper submission**: September 9, 2016

### Conference Steering Committee

<table>
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<th>Tadahiro KURODA, Keio Univ., Japan</th>
<th>kuroda [at] elec.keio.ac.jp</th>
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<td>Chair</td>
<td>Nobuo HAYASAKA, Toshiba, Corp., Japan</td>
<td>nobuo.hayasaka [at] toshiba.co.jp</td>
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<th>Chair</th>
<th>Yoshiro MASUBUCHI, Toshiba, Corp., Japan</th>
<th>yoshio.masubuchi [at] toshiba.co.jp</th>
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<tr>
<td>Chair</td>
<td>Deog-Kyoon JEONG, Seoul National Univ, Korea</td>
<td>dkjeong [at] snu.ac.kr</td>
</tr>
<tr>
<td>Co-Chair</td>
<td>Tsung-Hsien LIN, National Taiwan Univ.</td>
<td>thlin [at] ntu.edu.tw</td>
</tr>
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<td>Vice-Chair</td>
<td>Jaeha KIM, Seoul National Univ., Korea</td>
<td>jaeha [at] snu.ac.kr</td>
</tr>
<tr>
<td>Vice-co-Chair</td>
<td>Chia-Ihsiang YANG, National Taiwan Univ.</td>
<td>chyee [at] ntu.edu.tw</td>
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